AMENDMENTS TO THE CLAIMS

1. (Currently Amended) A system comprising:

a first device to detect a predetermined sequence of relevant data values indicating an event triggering command within a string of data values, said string of data values including said relevant data values and a number of non-relevant data values, wherein said predetermined sequence of relevant values is detected only if said string of data values includes no more than a finite nonzero number 'N' of non-relevant data values between any two sequential relevant data values.

2. (Original) The system of claim 1, further comprising a tap line to communicate said string of data values between a signal line and said first device.

3. (Previously Presented) The system of claim 2, wherein the event comprises a switching between a communication path between the first device and a second device and a communication path between the signal line and the second device.

4. (Previously Presented) The system of claim 3, wherein the first device is a logic device, the second device is a memory device, and said data values are memory addresses.

5. (Original) The system of claim 4, wherein the logic device is a Field Programmable Gate Array (FPGA).

6. (Original) The system of claim 4, wherein the memory device is Synchronous Dynamic Random Access Memory (SDRAM).

7. (Previously Presented) The system of claim 1, wherein said command is detected by a data value sequence detector.

8. (Original) The system of claim 7, wherein said detector includes a plurality of value sequencing units.

9. (Original) The system of claim 8, wherein each value sequencing unit includes at least one comparator communicatively coupled to at least one counter.

10. (Original) The system of claim 9, wherein each value sequencing unit is associated to a different relevant data value in the sequence of relevant data values.

11. (Previously Presented) The system of claim 10, wherein upon recognition of a first relevant data value in the sequence, by a first value sequencing unit associated to a first relevant data value, an associated first counter is to reset and then progress one counter state for each of a plurality of clocking signals, until 'N+2' counter states have passed by said first counter.

12. (Previously Presented) The system of claim 11, wherein, upon recognition of a second relevant data value, by an associated second value sequencing unit, before said first counter passes

'N+2' counter states, said second counter is to reset and then progress one counter state for each of said clocking signals, until 'N+2' counter states have passed by said second counter.

13. (Previously Presented) The system of claim 12, wherein, upon recognition of a third relevant data value, by an associated third value sequencing unit, before said second counter passes 'N+2' counter states, said third counter is to reset and then progress, one counter state for each of said clocking signals until 'N+2' counter states have passed by said second counter.

14. (Previously Presented) The system of claim 12, wherein upon recognition of a last relevant data value in the sequence after sequential recognition of all other relevant data values, the event-triggering command is to be detected.

15. (Currently Amended) A method comprising:

detecting a predetermined sequence of relevant data values indicating an event triggering command within a string of data values, said string of data values including said relevant data values and a number of non-relevant data values, wherein said predetermined sequence of relevant values is detected only if said string of data values includes no more than a finite nonzero number 'N' of non-relevant data values between any two sequential relevant data values.

16. (Original) The method of claim 15, wherein a tap line is to communicate said plurality of data values between a signal line and said first device.

17. (Previously Presented) The method of claim 16, wherein the event includes a switching

between a communication path between the first device and a second device and a communication path between the signal line and the second device.

18. (Previously Presented) The method of claim 17, wherein the first device is a logic device, the second device is a memory device, and said data values are memory addresses.

19. (Original) The method of claim 18, wherein the logic device is a Field Programmable Gate Array (FPGA) and the memory device is Synchronous Dynamic Random Access Memory (SDRAM).

20. (Previously Presented) The method of claim 15, wherein said command is detected by a data value sequence detector.

21. (Original) The method of claim 20, wherein said detector includes a plurality of value sequencing units.

22. (Original) The method of claim 21, wherein each value sequencing unit includes at least one comparator communicatively coupled to at least one counter.

23. (Original) The method of claim 22, wherein each value sequencing unit is associated to a different relevant data value in the sequence of relevant data values.

24. (Original) The method of claim 23, wherein upon recognition of a first relevant data value in the sequence, by a first value sequencing unit associated to a first relevant data value, an associated first counter resets and then progresses, one counter state for each of a plurality of clocking signals, until 'N+2' counter states have passed by said first counter.

25. (Original) The method of claim 24, wherein, upon recognition of a second relevant data value, by an associated second value sequencing unit, before said first counter passes 'N+2' counter state, said second counter resets and then progresses, one counter state for each of said clocking signals, until 'N+2' counter states have passed by said second counter.

26. (Original) The method of claim 25, wherein, upon recognition of a third relevant data value, by an associated third value sequencing unit, before said second counter passes 'N+2' counter states, said third counter resets and then progresses, one counter state for each of said clocking signals until 'N+2' counter states have passed by said second counter.

27. (Original) The method of claim 25, wherein upon recognition of a last relevant data value in the sequence after sequential recognition of all other relevant data values, the event-triggering command is perceived.

28. (Currently Amended) A system to perceive an event-triggering command, by a logic device, the system comprising:

a signal line to communicate a plurality of memory addresses between a host and one or more second devices; and

a logic device coupled to said signal line to detect a predetermined sequence of relevant memory addresses indicating the event triggering command within a string of memory addresses on said signal line, said string of memory addresses including said relevant memory addresses and a number of non-relevant memory addresses, wherein said predetermined sequence of relevant values is detected only if said string of memory addresses includes no more than a finite nonzero number 'N' of non-relevant memory addresses between any two sequential relevant memory addresses.

29. (Previously Presented) The system of claim 28, wherein the event comprises a switching between a communication path between the logic device and a memory device and a communication path between the signal line and the memory device.

30. (Original) The system of claim 29, wherein the logic device is a Field Programmable Gate Array (FPGA) and the memory device is Synchronous Dynamic Random Access Memory (SDRAM).